

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:
a first transistor;
an analog-to-digital converter coupled to the first transistor;
a digital encoder circuit coupled to receive output signals of the analog-to digital-converter; and
an impedance matching circuit coupled to receive output signals of the digital encoder circuit, wherein the impedance matching circuit comprises a plurality of second transistors coupled in parallel.

2. The integrated circuit of claim 1 wherein the first transistor is coupled to a resistor.

3. The integrated circuit of claim 1 wherein the impedance matching circuit is coupled in parallel with an I/O pin of the integrated circuit.

4. The integrated circuit of claim 1 wherein the impedance matching circuit is coupled in series with an I/O pin of the integrated circuit.

5. The integrated circuit of claim 4 wherein the impedance matching circuit is coupled to a buffer circuit that is coupled to the I/O pin.

6. The integrated circuit of claim 1 further comprising a plurality of impedance matching circuits coupled to receive output signals of the digital encoder circuit, wherein the plurality of impedance matching circuits each comprises a plurality of transistors coupled in parallel.

7. The integrated circuit of claim 1 wherein the analog-to-digital converter comprises a plurality of comparators that provide the analog-to-digital converter output signals.

8. The integrated circuit of claim 7 wherein the analog to digital

1 9. The integrated circuit of claim 1 wherein the plurality of second
2 transistors of the impedance matching circuit comprises four transistors coupled in parallel.

1 10. The integrated circuit of claim 1 wherein the plurality of second
2 transistors of the impedance matching circuit comprises five transistors coupled in parallel.

1 11. A method for providing impedance matching to a pin of an integrated
2 circuit using an impedance matching circuit, the method comprising:
3 generating a first signal in response to an impedance of a first transistor;
4 converting the first signal into a plurality of second signals; and
5 setting an impedance of the impedance matching circuit in response to the
6 plurality of second signals, wherein the impedance matching circuit is part of the integrated
7 circuit.

1 12. The method of claim 11 wherein generating the first signal comprises
2 generating the first signal from a resistor divider circuit that comprises the first transistor and
3 a resistor.

1 13. The method of claim 11 wherein converting the first signal in to a
2 plurality of second signals comprises converting the first signal into a plurality of digital
3 signals using an analog-to-digital converter.

1 14. The method of claim 13 wherein converting the first signal in to a
2 plurality of second signals further comprises converting the plurality of digital signals into
3 the plurality of second signals using a digital encoder circuit.

1 15. The method of claim 14 wherein the digital encoder circuit converts
2 the digital signals into the plurality of second signals that are a binary bit representation of the
3 digital signals.

1 16. The method of claim 11 wherein setting the impedance of the
2 impedance matching circuit further comprises causing each one of a plurality of second
3 transistors to be ON or OFF in response to the plurality of second signals.

1 17. The method of claim 16 wherein the plurality of second transistors
2 comprises at least four transistors coupled in parallel.

End of Page 4

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1 18. The method of claim 11 wherein the impedance matching circuit
2 comprises at least five transistors coupled in parallel.

1 19. The method of claim 11 wherein setting the impedance of the
2 impedance matching circuit further comprises setting the impedance of a plurality of
3 impedance matching circuits wherein each one of the plurality of impedance matching
4 circuits comprises a plurality of transistors coupled in parallel.

1 20. The method of claim 19 wherein the plurality of impedance matching
2 circuits are coupled in series or in parallel with respect to an associated I/O pin of the
3 integrated circuit.

1 21. An integrated circuit comprising:
2 programmable logic circuitry;
3 a first transistor for generating an analog signal;
4 circuitry for generating a plurality of digital signals in response to the analog
5 signal, wherein the circuitry includes an analog-to-digital converter, and the digital signals
6 comprise a binary representation of the analog signal; and
7 an impedance matching circuit comprising a plurality of second transistors,
8 wherein each of the second transistors is coupled to receive one of the digital signals.

1 22. The integrated circuit of claim 21 further comprising a plurality of
2 impedance matching circuits, each comprising a plurality of transistors that are each coupled
3 to receive one of the digital signals.

1 23. The integrated circuit of claim 22 wherein each of the impedance
2 matching circuits are associated with an I/O pin of the integrated circuit.

1 24. The integrated circuit of claim 23 wherein a subset of the impedance
2 matching circuits are coupled to a buffer circuit.

1 25. The integrated circuit of claim 23 wherein a subset of the impedance
2 matching circuits are coupled in parallel with an associated one of the I/O pins.

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27. The integrated circuit of claim 21 wherein the first transistor is coupled to an off-chip resistor, and wherein the first transistor and the off-chip resistor form a resistor divider.

28. The integrated circuit of claim 21 wherein the plurality of second transistors comprises at least four transistors coupled in parallel.

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